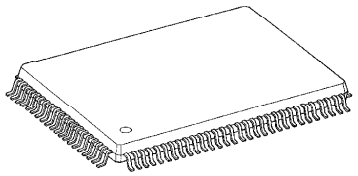
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A11F

MULTI SYSTEM 3DIM. DNR IC (FOR VCR)

TC90A11F is the digital video signal processor, which reduces the noise on the playback video signal of VCR, with the external video memory IC (2Mbit FIFO type). This IC is available for NTSC, PAL, etc. in world wide area.



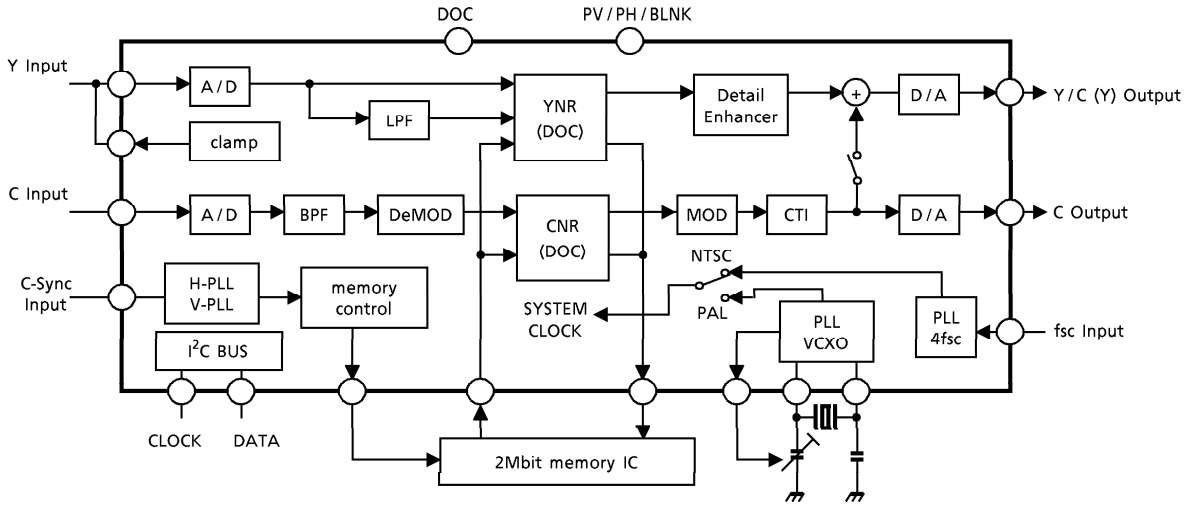
QFP100-P-1420-0.65A

Weight : 1.1g (Typ.)

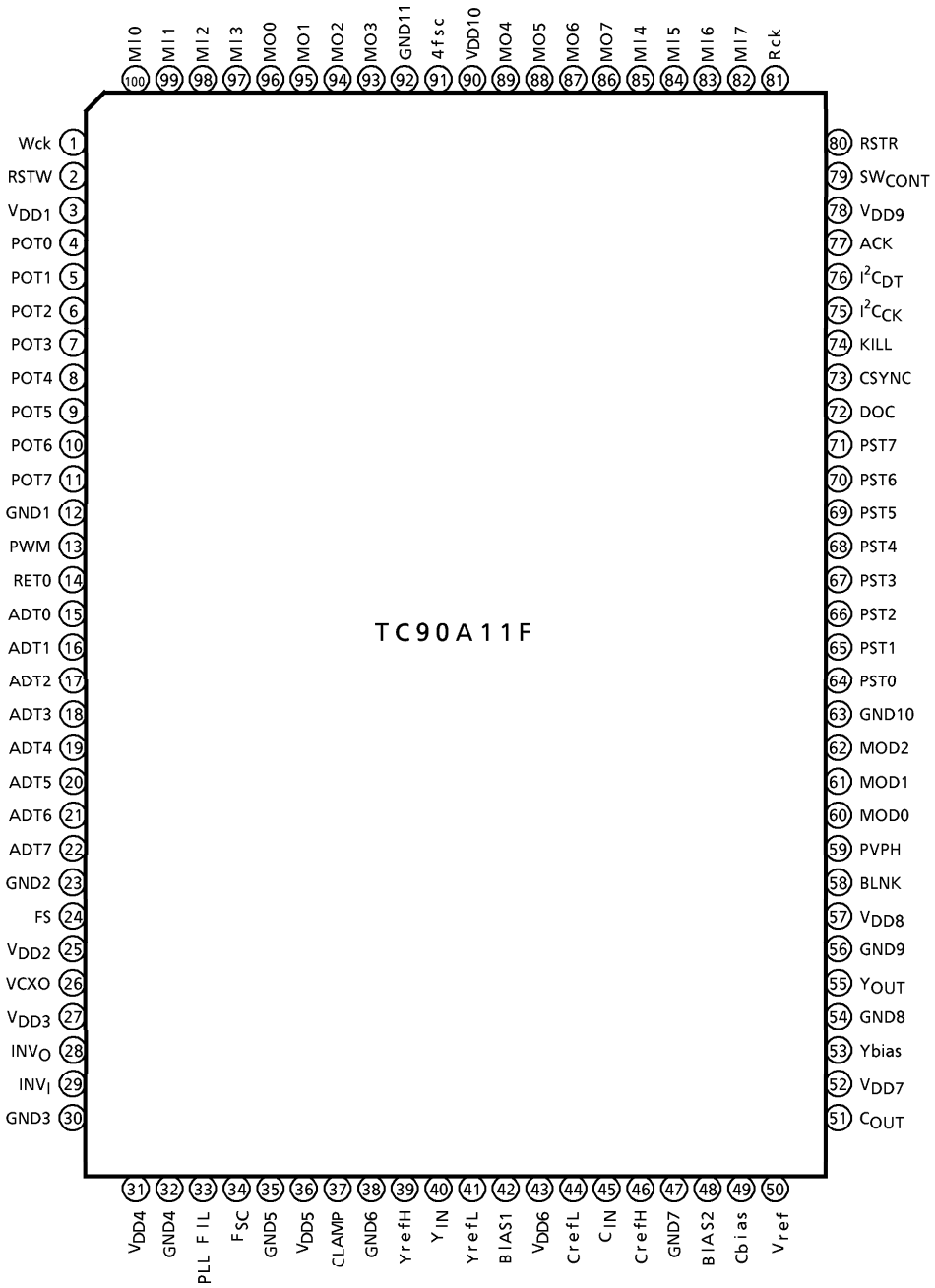
FEATURES

- Built-in 2 channels A / D converters. (for Luma & for Chroma)
- Built-in 2 channels D / A converters. A channel can be selected the output signal, Luma (Y) or Y / C mix. The other is for chroma output signal.
- Multi system, NTSC (3.58MHz, 4.43MHz), PAL and NTSC on PAL. (applying YNR only at SECAM)
- Built-in the clock generaters.
  at NTSC : ×4 PLL of fsc (chroma subcarrier frequency)
  at PAL : VCXO circuit locked the color burst.
- Built-in the digital H-PLL circuit and the digital V-PLL circuit.
- 3 kinds of NR system, Frame comb (NTSC only), Field comb, Line comb (for Trick mode).
- Applicable 2Mbit memory IC : μPD42280 (NEC), MSM518221
- Built-in the digital CTI (color detail enhancer)
- I^2C control

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

PIN No.	NAME	I/O	FUNCTION	REMARKS
1	Wck	Output	Writing clock to memory IC	High level>2.4V, low level<0.6V
2	RSTW	Output	Write reset pulse to memory	High level>2.4V, low level<0.6V
3	V_{DD1}	—	Digital voltage supply (5V)	—
4	POT0	Output	Output of test monitor	Output high level>2.4V, Output low level<0.6V
5	POT1	Output		
6	POT2	Output		
7	POT3	Output		
8	POT4	Output		
9	POT5	Output		
10	POT6	Output		
11	POT7	Output		
12	GND1	—	Digital GND	—
13	PWM	Output	VCXO control output	High level>2.4V, low level<0.6V
14	RETO	Input	Reset pin of internal logic	—
15	ADT0	Input	Pulse input for testing	Threshold of high level<2.4V Threshold of low level>0.8V
16	ADT1	Input		
17	ADT2	Input		
18	ADT3	Input		
19	ADT4	Input		
20	ADT5	Input		
21	ADT6	Input		
22	ADT7	Input		
23	GND2	—	Digital GND	—
24	FS	Input	Clock input (for VCXO)	Internal DC BIAS, minimum input level<$1V_{p-p}$
25	V_{DD2}	—	Digital GND	—
26	VCXO	Output	Buffer output of VCXO	Threshold (high)<2.4V, Threshold (low)>0.6V
27	V_{DD3}	—	Voltage supply of VCXO	—
28	INV_O	Output	Inverter output of VCXO	—
29	INV_i	Input	Inverter input of VCXO	—
30	GND3	—	GND of VCXO	—
31	V_{DD4}	—	Voltage supply of ×4 PLL	Recommend digital voltage supply (5V)
32	GND4	—	GND of ×4 PLL	Recommend digital GND
33	PLL FIL	—	Loop filter of ×4 PLL	—
34	F_{SC}	Input	Fsc input for ×4 PLL	Internal DC BIAS, minimum input level<$1V_{p-p}$
35	GND5	—	GND of AD converter	Recommend analog GND
36	V_{DD5}	—	Voltage supply of AD conv.	Recommend analog voltage supply (5V)
37	CLAMP	Output	CLAMP BIAS for Y input	$3/10 \times V_{DD}$ (5V)
38	GND6	—	GND of AD converter	Recommend analog GND
39	YrefH	—	High level REF. for Y-ADC	—
40	Y_{IN}	Input	Y (Luma) input	Typ. input : $1.6V_{p-p}$, signal CLAMP by pin 37

PIN No.	NAME	I/O	FUNCTION	REMARKS
41	YrefL	—	Low level REF. for Y-ADC	—
42	BIAS1	—	BIAS of AD converter	Common to Y-ADC and C-ADC
43	V_{DD6}	—	Voltage supply of AD conv.	Recommend analog voltage supply (5V)
44	CrefL	—	Low level REF. for C-ADC	—
45	C_{IN}	Input	C (Chroma) input	External BIAS : 1/2 V_{DD}, Typ. input : 1.14V_{p-p}
46	CrefH	—	High level REF. for C-ADC	—
47	GND7	—	GND of AD converter	Recommend analog GND
48	BIAS2	—	BIAS of DA converter	—
49	Cbias	—	BIAS of C-DAC	—
50	V_{ref}	—	Reference voltage of DAC	—
51	C_{OUT}	Output	C (Chroma) output	ON/OFF (fix to V_{DD}) controlled by BUS data
52	V_{DD7}	—	Voltage supply of DA conv.	Recommend analog voltage supply (5V)
53	Ybias	—	BIAS of Y-DAC	—
54	GND8	—	GND of DA converter	Recommend analog GND
55	Y_{OUT}	Output	Y (Luma) or Y/C output	ON/OFF (fix to V_{DD}), Y/C mix ON/OFF controlled by BUS
56	GND9	—	Digital GND	—
57	V_{DD8}	—	Digital voltage supply (5V)	—
58	BLNK	Input	Chroma mute (ON/OFF by BUS)	VTH : 1/6 V_{DD}, Lo = mute ON (for OSD character)
59	PVPH	Input	Chroma mute (ON/OFF by BUS)	VTH : 1/2 V_{DD}, Hi = mute ON (for SYNC period)
60	MOD0	Input	Test mode select	—
61	MOD1	Input		
62	MOD2	Input		
63	GND10	—	Digital GND	—
64	PST0	Input	Test signal input	Threshold of high level < 2.4V Threshold of low level > 0.8V
65	PST1	Input		
66	PST2	Input		
67	PST3	Input		
68	PST4	Input		
69	PST5	Input		
70	PST6	Input		
71	PST7	Input		
72	DOC	Input	DOC pulse input	< 0.8V → DOC ON, > 2.4V → OFF
73	CSYNC	Input	C-SYNC input	VTH : < 2.4V / > 0.8V, hysteresis : 0.4V
74	KILL	Input	Color killer	> 2.4V → killer ON, < 0.8V → OFF
75	I^2C_{CK}	Input	Click input of I^2C BUS	VTH : < 2.4V / > 0.8V, hysteresis : 0.4V
76	I^2C_{DT}	Input	Data input of I^2C BUS	—
77	ACK	Output	Acknowledge output I^2C BUS	High level > 2.4V, low level < 0.6V
78	V_{DD9}	—	Digital voltage supply (5V)	—
79	SW_{CONT}	Output	BUS decode output	High level > 2.4V, low level < 0.6V
80	RSTR	Output	Read reset pulse to memory	High level > 2.4V, low level < 0.6V

PIN No.	NAME	I/O	FUNCTION	REMARKS
81	Rck	Output	Reading clock to memory IC	High level>2.4V, low level<0.6V
82	MI7	Input	Data input from memory IC	Threshold of high level<2.4V Threshold of low level>0.8V
83	MI6	Input		
84	MI5	Input		
85	MI4	Input		
86	MO7	Output	Data output to memory IC	Output high level>2.4V, Output low level<0.6V
87	MO6	Output		
88	MO5	Output		
89	MO4	Output		
90	V_{DD10}	—	Digital voltage supply (5V)	—
91	4fsc	Output	System clock monitor	High level>2.4V, low level<0.6V
92	GND11	—	Digital GND	—
93	MO3	Output	Data output to memory IC	Output high level>2.4V, Output low level<0.6V
94	MO2	Output		
95	MO1	Output		
96	MO0	Output		
97	MI3	Input	Data input from memory IC	Threshold of high level<2.4V Threshold of low level>0.8V
98	MI2	Input		
99	MI1	Input		
100	MI0	Input		

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~+6.0	V
Input Voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Power Dissipation	P_D (Note)	1.75	W
Operating Temperature	T_{opr}	−10~75	°C
Storage Temperature	T_{stg}	−40~125	°C

(Note) Ta = 25°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = – 10~75°C, V_{DD} = 4.75~5.25V)

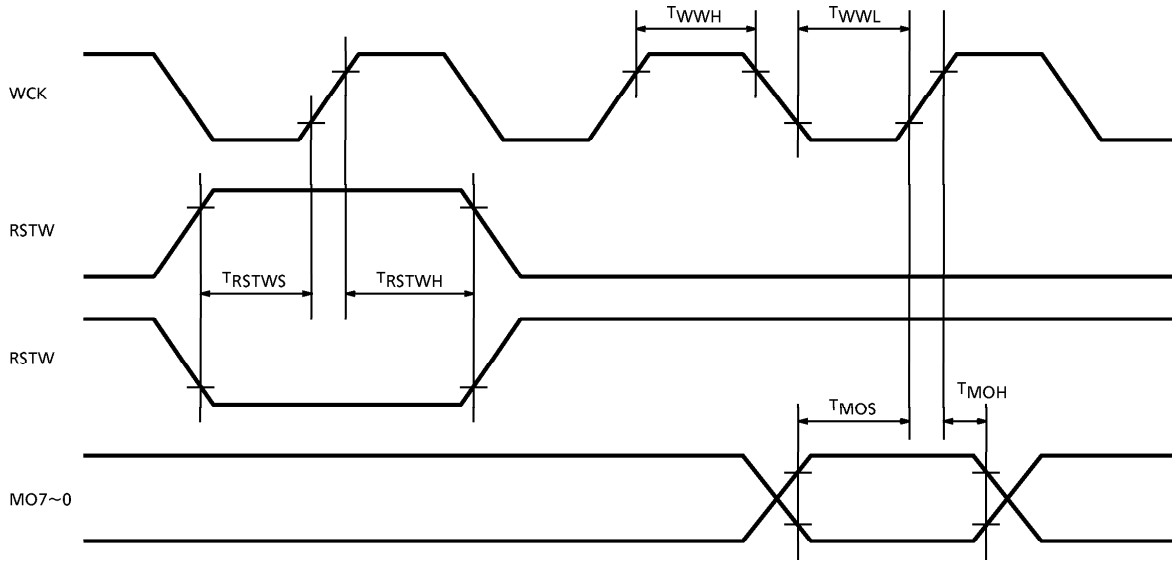
CHARACTERISTIC	PIN	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	—	I_{DD}	—	—	—	165	mA
Threshold of High Level	(*A)	V_{IH1}	—	2.4	—	—	V
	(*B)	V_{IH2}	—	2.4	—	—	
	(*C)	V_{IH3}	—	4.0	—	—	
	59 (PV / PH)	V_{IH4}	—	$1/2V_{DD}+0.3$	—	—	
	58 (BLNK)	V_{IH5}	—	$1/6V_{DD}+0.2$	—	—	
Threshold of Low Level	(*A)	V_{IL1}	—	—	—	0.8	V
	(*B)	V_{IL2}	—	—	—	0.8	
	(*C)	V_{IL3}	—	—	—	1.0	
	59 (PV / PH)	V_{IL4}	—	—	—	$1/2V_{DD}-0.3$	
	58 (BLNK)	V_{IL5}	—	—	—	$1/6V_{DD}-0.2$	
Input Current (High)	(*A), (*B), (*C)	I_{IH1}	—	– 10	—	+ 10	μA
Input Current (Low)	(*A), (*B), (*C)	I_{IH2}	—	– 10	—	+ 10	μA
Output High Level	—	V_{OH}	I_{OH} = – 4mA	2.4	—	—	V
Output Low Level	—	V_{OL}	I_{OL} = 4mA	—	—	0.6	V
Hysteresis Level	—	V_{HS}	—	—	0.4	—	V

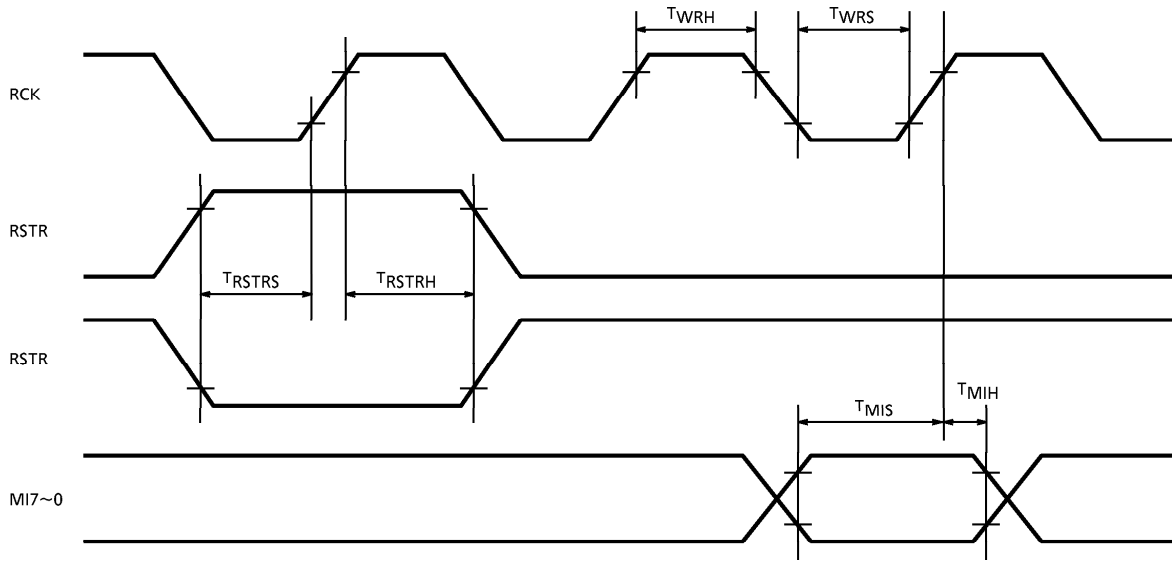
(*A) 15 – 22, 64, 72, 74, 82, 85, 97, 100
(*B) 73, 75
(*C) 14, 60 – 62

AC CHARACTERISTICS (Ta = 25°C, V_{DD} = 5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Level (Y)	Yin	White 100% at pin 40	—	1.6	2.0	V_{p-p}
Input Level (C)	Cin	100 IRE Chroma at pin 45	—	1.15	2.0	V_{p-p}
Fsc (Pin 34) Input Level	Lsc	Sine wave at pin 34	0.3	1.0	2.0	V_{p-p}
Operation Frequency Range	Fsc	$1.0V_{p-p}$ sine wave at pin 34	3.47	3.58 / 4.43	4.58	MHz
FS (Pin 24) Input Level	Lfs	—	1.0	—	—	V
Input Range of AD Conv.	AD IN	Pin 40, pin 45	3 / 10 V_{DD}	—	7 / 10 V_{DD}	V
Output Signal Level at Pin 55	Y_{out}	Yin = $1.6V_{p-p}$ V_{ref} = 2.5V (pin 50)	—	2.0	—	V_{p-p}
Output Chroma Level at Pin 55 & Pin 51	C_{out}	Cin = $1.15V_{p-p}$ V_{ref} = 2.5V (pin 50)	—	1.43	—	V_{p-p}
Output Impedance	Zo	—	200	350	700	Ω
Set Up Period to Read the Data of Memory	T_{MIS}	—	25	—	—	ns
Hold Period to Read the Data of Memory	T_{MIH}	—	3	—	—	ns
Clock Pulse Width to Memory IC	T_{WRH}	Load impedance : 15pF	20	—	—	ns
	T_{WRL}		20	—	—	
	T_{WWH}		20	—	—	
	T_{WWL}		20	—	—	
Pulse Timing to Memory IC	T_{RSTRS}	—	15	—	—	ns
	T_{RSTRH}		10	—	—	
	T_{RSTWS}		15	—	—	
	T_{RSTWH}		10	—	—	
	T_{MOS}		15	—	—	
	T_{MOH}		10	—	—	

TIMING CHART

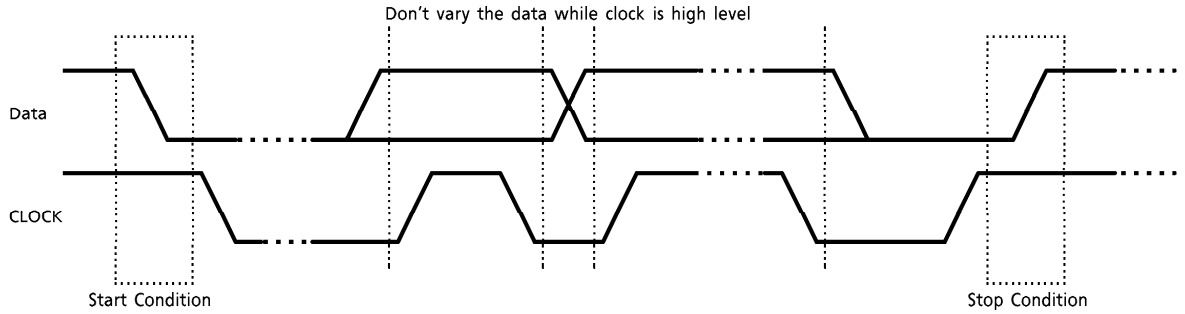




I²C-BUS OUTLINE

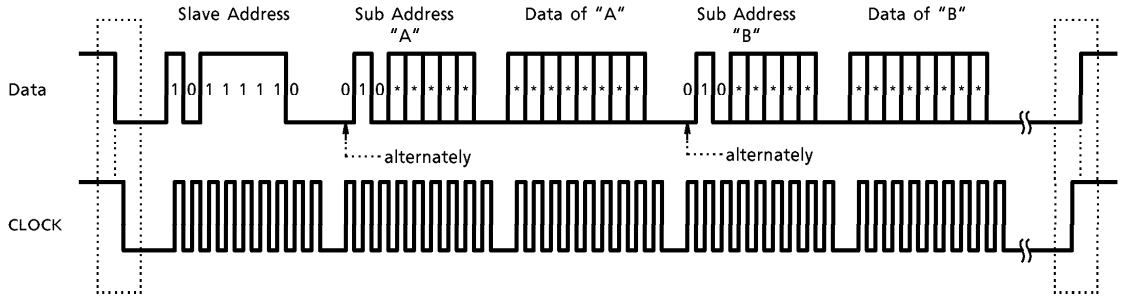
The I²C-BUS has two wires, serial data (SDA) and serial clock (SCL) which carry information between the IC's are connected to the bus line. The bus is considered to be busy after the "Start Condition". The bus is considered to be free again after the "Stop Condition".
A HIGH to LOW transition of the SDA line while SCL is HIGH, defines a Start Condition.
A LOW to HIGH transition of the SDA line while SCL is HIGH, defines a Stop Condition.
Every bytes put on the SDA line must be 8bit long. Each byte has to be followed by acknowledge bit. Each SDA and SCL has to be pulled up the voltage supply via a resistor.

DON'T ..... Don't vary the data while clock is high level at data transmission.

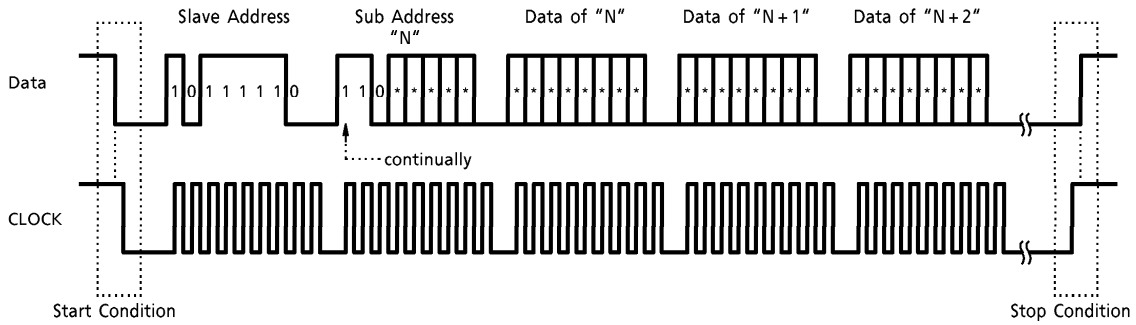


This IC adopts the sub address format. Send the sub address and the data alternately after the slave address. If the first bit of the sub address which is sent first is changed to "1", some data can be sent continually. (Refer to follow)

INPUT SUB ADD. AND DATA ALTERNATELY



INPUT DATA CONTINUALLY AFTER SUB ADD.



CONTENTS OF BUS LINE CONTROL

Table of I^2C BUS control

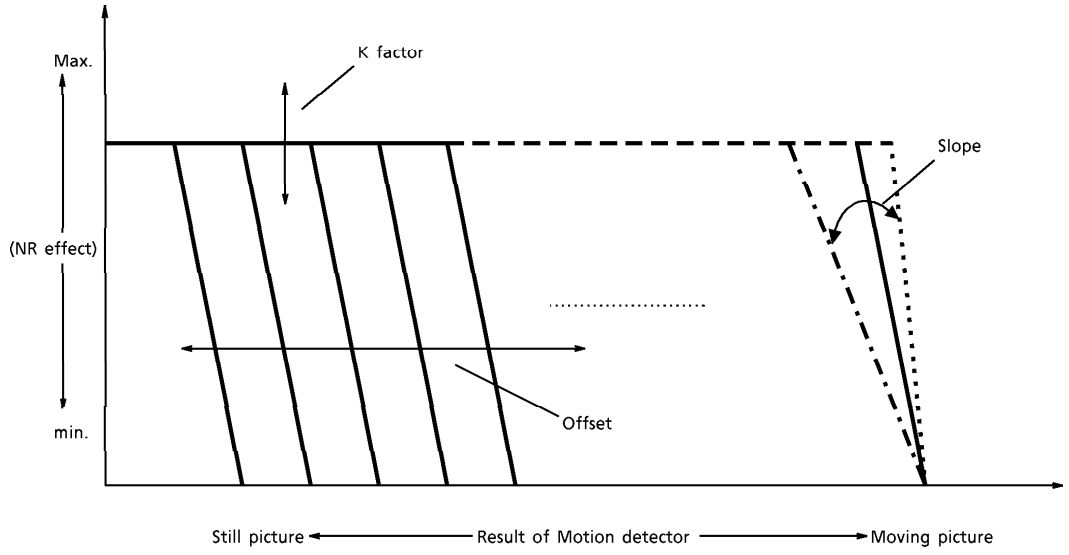
Slave address = (10111110)

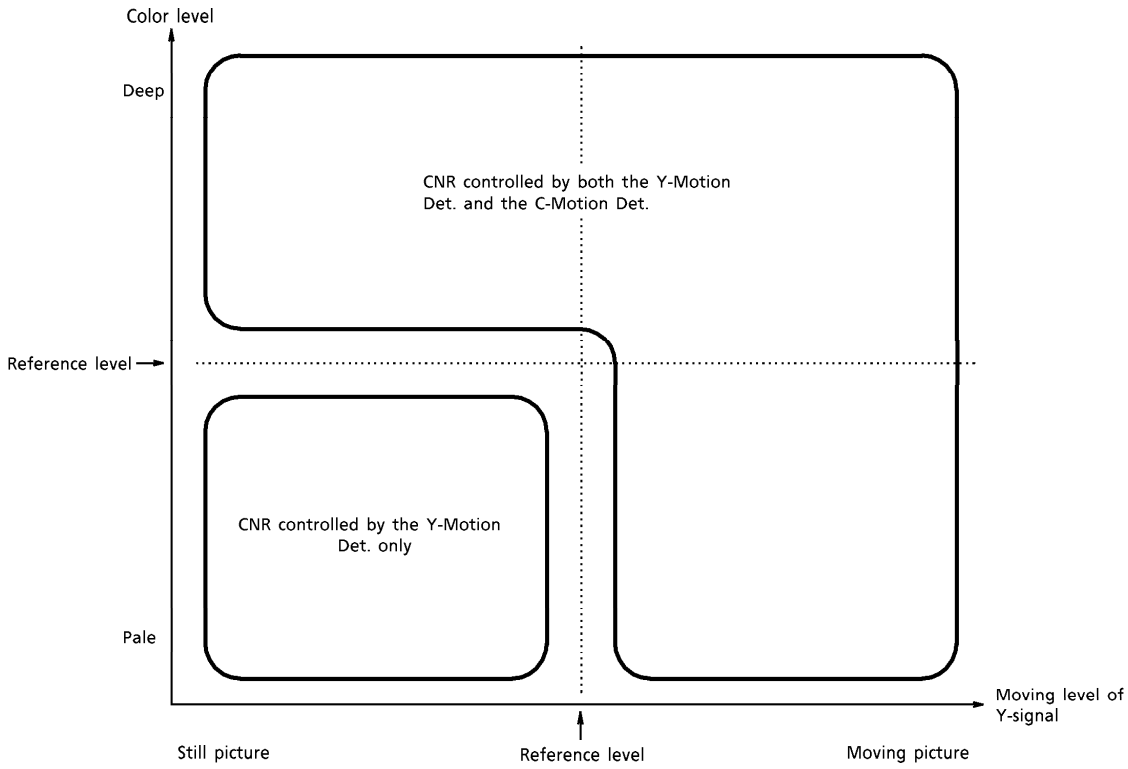
SUB ADD.	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
40	K factor of YNR				Limiter level of YNR			
41	K factor of CNR				Limiter level of CNR			
42	Offset of Y motion detector for YNR				Slope of Y det. for YNR		0 (None)	0 (None)
43	Offset of Y motion detector for CNR				Slope of Y det. for CNR		0 (None)	0 (None)
44	Offset of C motion detector for CNR				Slope of C det. for CNR		0 (None)	0 (None)
45	Y motion det. reference level for cross color				Chroma reference level for cross color			
46	Motion detector OFF (still)			Y-mot. wide	0 (TEST)	NR OFF	0 (TEST)	443NTSC
47	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	Mod. OFF
48	Delay of chroma mute for BLNK pulse					C-Mute OFF	Y / C DELAY	0 (TEST)
49	0 (TEST)	0 (TEST)	Timing adjustment of the delayed signal from memory					
4A	PAL	Timing adjustment between video signal and C-sync						
4B	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	1 (TEST)	0 (TEST)
4C	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (Fix)	Memory IC	Field / frame
4D	0 (TEST)	SW Control	0 (TEST)	0 (TEST)	0 (TEST)	0 (Fix)	0 (TEST)	0 (TEST)
4E	0 (Fix)	0 (TEST)	0 (TEST)	0 (Fix)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)
4F	Y-DOC	C-DOC	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	BPF OFF	0 (TEST)
50	0 (TEST)	1 (Fix)	Standard / non Standard		SW CLK in	VCXO OFF	PLL OFF	1 (Fix)
51	50Hz / 60Hz	4.43 / 3.58	line NR	V mask position for brst PLL			0 (TEST)	1 (TEST CLR)
52	Burst gate position for VCXO							1 (Fix)
53	C-NC ON	Limiter level of C-NC		Y-DAC ON	C-DAC ON	PV / PH OFF	0 (TEST)	0 (TEST)
54	Delay of Y signal		Delay of C signal		0 (Fix)	1 (Fix)	DeMod. OFF	Y / C Mix / Sep
55	0 (TEST)	0 (TEST)	0 (Fix)	0 (Fix)	0 (Fix)	PAL / NTSC	0 (TEST)	0 (TEST)
56	Y detail enhanced level		C-enh. det.	0 (Fix)	C detail enhanced level		C-enh. OFF	0 (TEST)
57 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)
58 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (None)	0 (None)
59 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (None)	0 (TEST)	0 (TEST)
5A (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (None)	0 (None)	0 (None)	0 (None)	0 (TEST)
5B (TEST)	0 (TEST)	0 (None)	0 (TEST)	0 (TEST)	0 (TEST)	0 (None)	0 (TEST)	0 (TEST)
5C (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)
5D (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)	0 (TEST)

DETAIL EXPLANATION OF BUS CONTROL

1. Motion detector function and the setting of BUS bit

- Motion detectors decide the picture (part) is near the moving or the still by detecting the differential level between the input signal and the delayed signal (a frame or a field).
- The NR circuit receives the result of motion detectors and makes the "K factor" reduce to "0" (NR OFF) at the parts of the moving picture.
- The middle range of "K factor" have 5 steps from the setting value to "0", and the offset value, which is the starting point to reduce the "K factor", and slope is programmable by I^2C BUS control.
- YNR is controlled by the Y-motion detector only, and CNR is controlled by both the Y-motion detector and the C-motion detector. But in case of that the color level is small and the motion of Y-signal is small, CNR is controlled by only the Y-motion detector to decrease the cross color component.





- BUS control data

① K factor of YNR (Sub address 40H ; D_7~D_4)

K factor can be changed by 14 steps from 0 to maximum. K factor of YNR increases in proportion to the setting data of these bits.

② Limiting level of YNR (Sub address 40H ; D_3~D_0)

The limiting level can be changed by 16 steps from 0 to maximum. Limiting level of YNR increases in proportion to the setting data of these bits.

③ K factor of CNR (Sub address 41H ; D_7~D_4)

K factor can be changed by 14 steps from 0 to maximum. K factor of CNR increases in proportion to the setting data of these bits.

④ Limiting level of CNR (Sub address 41H ; D_3~D_0)

The limiting level can be changed by 16 steps from 0 to maximum. Limiting level of CNR increases in proportion to the setting data of these bits.

⑤ Offset of Y motion detector for YNR (Sub address 42H ; D_7~D_4)

This data can be changed by 16 steps from 0 to maximum. When the data is smaller, the motion detector make the K factor of YNR reduce more near the still picture, so, YNR effect is smaller. Conversely when the data is bigger, K factor doesn't decrease more near the moving picture, so, the afterimage comes into view on the moving picture.

⑥ Slope of Y motion detector for YNR (Sub address 42H ; D_3, D_2)

This data can be changed by 3 steps.
"00" = steep slope, "01" = middle, "10" = gentle slope

⑦ Offset of Y motion detector for CNR (Sub address 43H ; D_7~D_4)

This data can be changed by 16 steps from 0 to maximum. When the data is smaller, the motion detector make the K factor of CNR reduce more near the still picture, so, CNR effect is smaller. Conversely when the data is bigger, K factor doesn't decrease more near the moving picture, so, the color blur increases on the moving picture.

⑧ Slope of Y motion detector for CNR (Sub address 43H ; D_3, D_2)

This data can be changed by 3 steps.
"00" = steep slope, "01" = middle, "10" = gentle slope

⑨ Offset of C motion detector for CNR (Sub address 44H ; D_7~D_4)

This data can be changed by 16 steps from 0 to maximum. When the data is smaller, the motion detector make the K factor of CNR reduce more near the still picture, so, CNR effect is smaller. Conversely when the data is bigger, K factor doesn't decrease more near the moving picture, so, the afterimage comes into view on the moving picture.

⑩ Slope of C motion detector for CNR (Sub address 44H ; D_3, D_2)

This data can be changed by 3 steps.
"00" = steep slope, "01" = middle, "10" = gentle slope

⑪ Reference level of Y motion detector for cross color (Sub address 45H ; D_7~D_4)

This data can be changed by 16 steps. When the data is bigger, the countermeasure effect of the cross color works more near the moving picture.

⑫ Reference level of Y motion detector for cross color (Sub address 45H ; D_3~D_0)

This data can be changed by 16 steps. When the data is bigger, the countermeasure effect of the cross color works to the bigger color signal level.

⑬ ON / OFF of Y motion detector for YNR (Sub address 46H ; D_7)

Y motion detector for YNR is forced OFF at "1". (YNR is always ON.)

⑭ ON / OFF of Y motion detector for CNR (Sub address 46H ; D_6)

Y motion detector for CNR is forced OFF at "1".
(CNR is controlled by only C motion detector.)

⑮ ON / OFF of C motion detector for CNR (Sub address 46H ; D_5)

C motion detector for CNR is forced OFF at "1".
(CNR is controlled by only Y motion detector.)

⑯ Wide mode of the moving picture part (Sub address 46H ; D_4)

The moving picture parts widen for ±2 cycle of clock at "1".

⑰ The moving picture parts to black (Sub address 46H ; D3) ..... (Test mode)

The moving picture parts is replaced to black by the result of motion detector at "1".

Y motion detector result (Sub Address $4F_H$; D_5) = "1"

C motion detector result (Sub Address $4F_H$; D_5) = "1"

This function is only for the evaluation. Don't use this function for the other aim,

⑱ YNR and CNR OFF (Sub address 46H ; D_2)

The result of all motion detectors is replaced to the moving picture at "1".
(YNR and CNR is always OFF.)

2. The setting of BUS for the television standards

SUB ADD	DATA	CONTROL ITEM	"0"	"1"	NTSC	443NTSC	PAL	SECAM	S-VHS (NTSC)
46	D_0	443NTSC	358NTSC	443NTSC	0	1	0	1	0
47	D_0	De-mod OFF	NORMAL	OFF	0	0	0	1	0
4A	D_7	PAL	NTSC	PAL	0	0	1	0	0
4F	D_1	BPF OFF	NORMAL	THROUGH	0	0	0	1	0
50	D_3	SW CLK in	FS	Fsc	1	1	0	1	1
50	D_2	VCXO OFF	ACT	STOP	1	1	0	1	1
50	D_1	PLL OFF	ACT	STOP	0	0	1	0	0
51	D_7	50 / 60	60Hz	50Hz	0	0	1	1	0
51	D_6	4.43 / 3.58	3.58MHz	4.43MHz	0	1	1	1	0
53	D_3	C-DAC ON	OFF	ON	0	0	0	0	1
54	D_1	Mod OFF	NORMAL	OFF	0	0	0	1	0
54	D_0	Y / C mix OFF	Y-ONLY	YC-MIX	1	1	1	1	0
55	D_2	PAL / NTSC	PAL	NTSC	—	1	0	—	—

① 443NTSC (Sub address 46H ; D_0)

VCO frequency of the 4fsc PLL is changed by this bit.

0 : fsc = 3.58MHz, 1 : fsc = 4.43MHz

② De-modulation OFF (Sub address 47H ; D_0)

The chroma demodulator is ON / OFF by this bit. Select OFF at only SECAM mode.

0 : ON, 1 : OFF

③ PAL (Sub address 4AH ; D_7)

The chroma modulating and de-modulating system is selected by this bit.

0 : NTSC, 1 : PAL

④ BPF OFF (Sub address 4FH ; D_1)

The chroma BPF is ON / OFF by this bit. Select OFF at only SECAM mode.

0 : ON, 1 : OFF

⑤ Switch of the clock input (Sub address 50H ; D_3)

The clock input terminal is selected by this bit.

0 : pin 24 (for VCXO), 1 : OFF : pin 34 (for 4fsc PLL)

⑥ VCXO OFF (Sub address 50H ; D_2)

The VCXO driver of the burst PLL is ON / OFF by this bit.

0 : ON, 1 : OFF

⑦ PLL OFF (Sub address 50H ; D_1)

The 4fsc PLL is ON / OFF by this bit.

0 : ON, 1 : OFF

⑧ 50Hz / 60Hz (Sub address 51H ; D_7)

This bit is for selection of the field frequency.

0 : 60Hz, 1 : 50Hz

⑨ 4.43MHz / 3.58MHz (Sub address 51H ; D_6)

This bit is for selection of the system clock frequency by fsc.

0 : fsc = 3.58MHz, 1 : fsc = 4.43MHz

⑩ C-DAC ON (Sub address 53H ; D_3)

Chroma output (at Pin 51) is ON / OFF by this bit.

0 : OFF, 1 : ON

⑪ Modulation OFF (Sub address 54H ; D_1)

The chroma modulator is ON / OFF by this bit. Select OFF at only SECAM mode.

0 : ON, 1 : OFF

⑫ Y / C mix OFF (Sub address 54H ; D_0)

This bit is for selection of the output signal at Pin 55, composite video (Y / C) or Luma only (Y).

0 : Y / C mix, 1 : Y only

⑬ PAL / NTSC (Sub address 55H ; D_2)

This bit is for selection of the detection system of burst PLL, NTSC or PAL. When you will only use the burst PLL at NTSC signal, set this bit "1".

0 : PAL, 1 : NTSC

⑭ SW control (Sub address 4DH ; D_6)

This bit is for the external SW control. Pin 79 (SW_{CONT}) is the decoding terminal of this bit.

0 : Low, 1 : High

(Note) When the bit of "Y-DAC ON" (Sub add 53H ; d4) is "1", the Y-DAC output terminal (Pin 55) is fixed "Hi" (near the V_{DD} level).

3. The adjustment of the internal logic timing by BUS data

① Delay of chroma mute for BLNK pulse (Sub address 48H ; D_7~D_3)

The color component of the output signal at Pin 51 (Cout) or / and Pin 55 (Yout) is OFF during Pin 74 (BLNK) is low. This color mute timing can be shifted by the data of these bits.

② Timing adjustment of the delayed signal from the memory IC (Sub address 49H ; D_5~D_0)

These bits are for the timing adjustment between the input signal and the delayed signal from the external memory IC. Normally, these bits are set as follows for each NR mode.

Field or Frame NR mode ..... 17H = (**010111)
Line NR mode ..... 08H = (**001000)

③ Timing adjustment of the video signal and the C-sync (Sub address 49H ; D_5~D_0)

To save the bits data for the memory IC, the NR effect is OFF except the picture parts of the video signal. This timing is made from the C-sync (Pin 73), and the horizontal position can be sifted by these bus bits data.
So, set the data for these bits to meet the timing between the action period of WCK (Pin 1) and the picture parts of internal video signal, that is 1μs later than the signal of Yin (Pin 40).

④ V mask position for burst PLL (Sub address 51H ; D_4~D_2)

The detector of the burst PLL stops during the Vertical Blanking period. This period can be selected by bus data. But, normally select the longest period ($D_4 = 0$, $D_3 = 1$).

Front of V mask period : "$D_4 = 0$" ; early, "$D_4 = 1$" ; late
End of V mask period : "(D_3, D_2) = (0, 0)" ; early
"(D_3, D_2) = (0, 1)" ; center
"(D_3, D_2) = (1, x)" ; late

⑤ Burst gate position for VCXO (Sub address 52H ; D_7~D_1)

The gate pulse of burst PLL is made from C-sync, so you have to adjust the timing of this pulse to the internal burst position, that is 500ns later than the signal of Cin (Pin 45). This gate pulse can be observed at Pin 13 (PWM) under the test mode as follows.

Test mode for the observation of the burst gate pulse
Sub Address 4BH ; $D_1 = 0$
Sub Address 4EH ; $D_6 = 1$
Sub Address 4EH ; $D_3 = 1$
Sub Address 55H ; $D_1 = 1$

⑥ Delay of Y signal (Sub address 54H ; D_7, D_6) (Note) Fix 0 at "Y / C Delay" = 1 (C delay mode)
Delay of C signal (Sub address 54H ; D_5, D_4) (Note) Fix 0 at "Y / C Delay" = 0 (Y delay mode)

These bits are for the adjustment of Y / C timing at output. First, select the Y delay or C delay by the bit of "Y, C Delay" (Sub Address 48H ; D_1).

4. The others

① Color mute control

The terminal who make the chroma output OFF is as follows.

- BLNK (Pin 58) ; Mute the color where is the characters at OSD super impose mode.
- PVPH (Pin 59) ; Mute the color where is vertical blanking period, because the color is not here.
- KILL (Pin 74) ; Make the color OFF when the input signal is the B / W signal.

The functions of BLNK (Pin 58) and PVPH (Pin 59) can be made OFF by bus control as follows.

- C-Mute OFF (Sub Address 48H ; D_2) = 1→BLNK (Pin 58) is ignored.
- PV / PH OFF (Sub Address 53H ; D_2) = 1→PVPH (Pin 59) is ignored.

② Memory IC (Sub address 4CH ; D_1)

0 : μPD42280 (by NEC), 1 : MSM518221 (by OKI)

③ Field / frame (Sub address 4CH ; D_0)

0 : Frame NR (NTSC only), 1 : Field NR

④ Standard / non standard (Sub address 50H ; D_5, D_4)

The video signal from the PC and the TV game etc. is different from the television standard. This IC detects the input signal is the standard or not, and usually makes the NR effect OFF automatically. But the manual select is available by bus control.

D_5 ; 0 : Automatic, 1 : BUS control (D_4)

D_4 ; 0 : Standard, 1 : Non-standard

(Note) On the trick mode of VCR, the input signal may be regarded as the non-standard because the number of lines in a field is different from on normal play back. If you need the (line) NR effect on the trick mode, you select the standard fix mode by bus.

⑤ Line NR (Sub address 51H ; D_5)

The line NR mode is usually used on the trick mode of VCR, because the field correlation is small in this case. This IC doesn't have the internal line memory, so the external memory is used on the line NR mode, too.

0 : Frame / Field NR, 1 : Line NR

⑥ Drop-out compensation

This IC have the function that replace the input signal by the delayed signal during low level at Pin 72 (DOC). But this function can not be used at the field / frame NR mode, because the delayed signal is noting at the sync parts. So you can use this function at the line NR mode only.

- Y-DOC (Sub Address 4FH ; D_7) = 1 .... Y signal component is replace by DOC pulse at Pin 72.
- C-DOC (Sub Address 4FH ; D_6) = 1 .... C signal component is replace by DOC pulse at Pin 72.

⑦ Chroma noise cancel

- C-N.C. ON (Sub Address 53H ; D_7)
  0 : OFF, 1 : ON
- Limiter level of C-N.C. (Sub Address 53H ; D_6, D_5)
  00 : 2, 10 : 4, 01 : 8, 11 : 16

⑧ Y detail enhanced level (Sub address 56H ; D_7, D_6)

00 : 0 (OFF), 01 : 0.25, 10 : 0.5, 11 : 1.0

⑨ C detail enhancer (Sub address 56H ; D_5, D_3, D_2, D_1)

This function is the enhancement of chroma signal level near the edge of Y signal.

- D_5 ; Edge detecting level ..... 0 : Low, 1 : High
- D_3, D_2 ; Enhancement level of the chroma detail
  00 : 0.5, 01 : 1.0, 10 : 1.5, 11 : 2.0
- D_1 ; C detail enhancer OFF
  0 : ON, 1 : OFF

DESIGNING FILTER CIRCUIT

a) Input low-pass filter

This low-pass filter is used to limit the frequency bandwidth of the input signal to below a half of the clock frequency. If the input signal contains a high frequency component and this input filter is not, it may interfere with clock frequency inside the IC, generating a frequency component that can be removed by an output filter. (Reflected distortion)

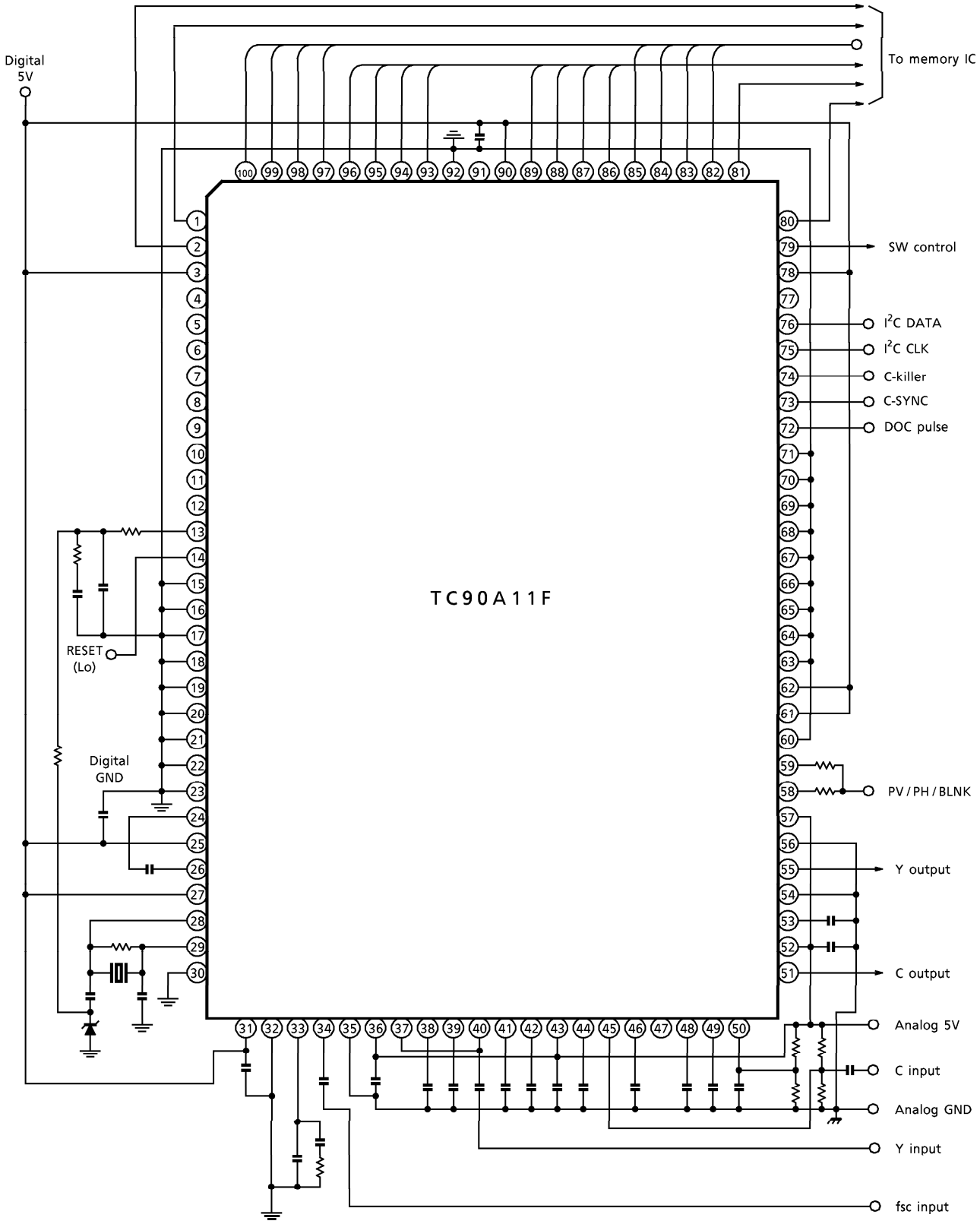
b) Output low-pass filter

This filter is used to remove clock frequency components (including harmonics) in the IC's output signal, as well as remove the reflected distortion at input.

CAUTION

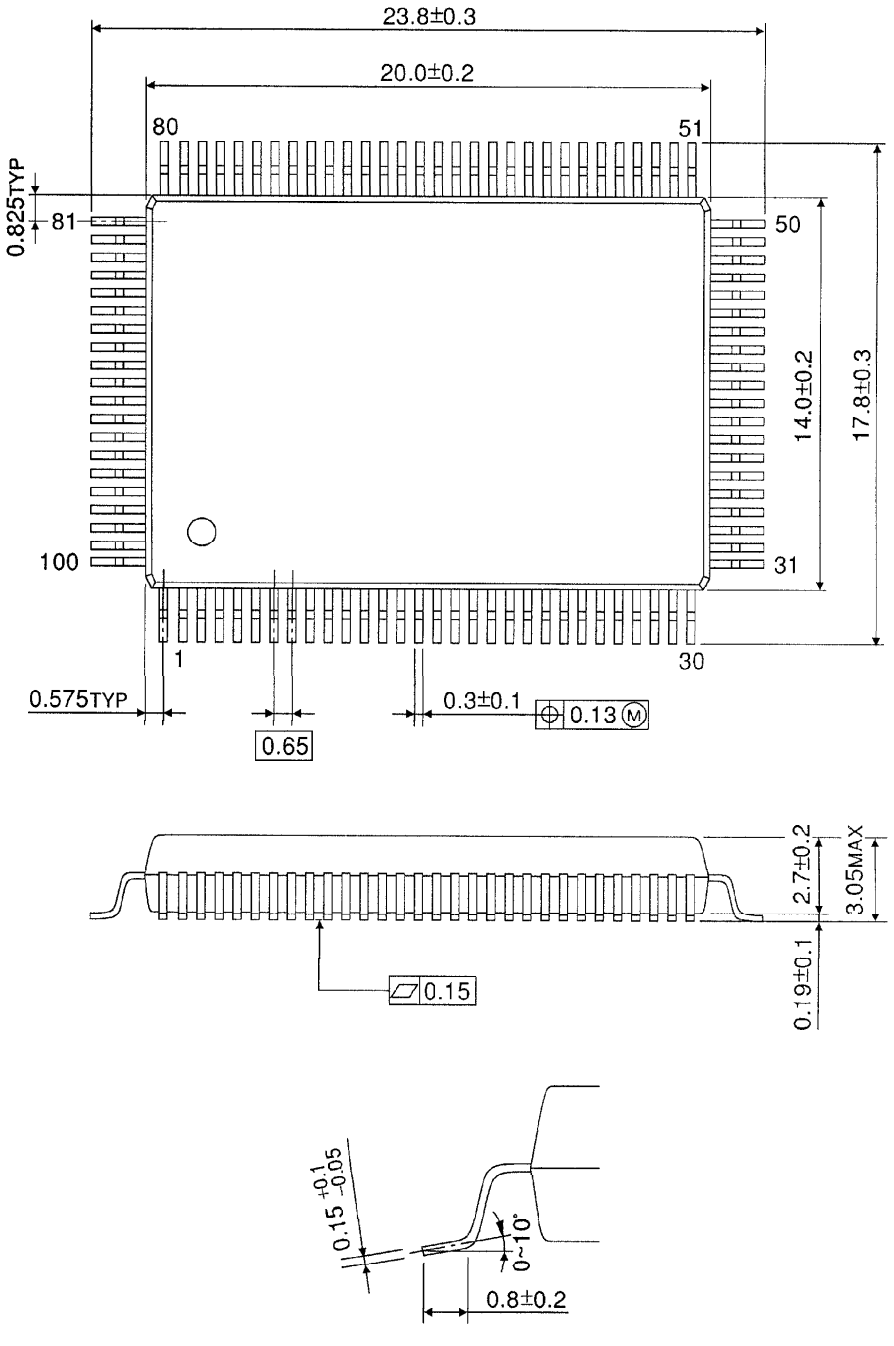
This device is electrostatic sensitive device, so care must be taken in handling and storage to prevent deterioration or damage by means of shorting electrically all pins with use of aluminum foil or conductive mat.
Even in assembled on board, it is necessary to protect against surge or inductive noise from input, output and power supply line.

APPLICATION CIRCUIT



OUTLINE DRAWING

QFP100-P-1420-0.65A Unit : mm



Weight : 1.1g (Typ.)